What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of controlling a power supply comprising:

reading a digital signal on a digital data bus;

generating a control signal in relation to said digital signal;

feeding said control signal forward to a power supply; and

modifying a power output of said power supply in response to said control signal in anticipation of a changing power demand of a load responsive to said digital signal.

2. A method of controlling a power supply as defined in claim 1 wherein said power supply further comprises a plurality of charge pump circuits and a respective plurality of clock generation circuits, each of said clock circuits operatively connected to, and adapted to drive, said respective charge pump circuit.

3. A method of controlling a power supply as defined in claim 2 further comprising:

enabling one of said plurality of clock circuits and thereby driving said respective charge pump circuit.

4. A method of controlling a power supply as defined in claim 1 wherein said digital data bus is configured as a parallel data bus.

5. A method of controlling a power supply as defined in claim 1 wherein said control signal is a digital signal.

6. A method of controlling a power supply as defined in claim 1 wherein said control signal is an analog signal.

7. A method of controlling a power supply as defined in claim 6 wherein said analog signal further comprises a voltage signal having a magnitude proportional to a multiple of data bits of a data word on said data bus having a particular state.

8. A method of controlling a power supply as defined in claim 7 wherein said multiple of data bits comprises four data bits.

9. A method of controlling a power supply as defined in claim 7 further comprising:

generating said voltage signal by flowing an electrical current through a voltage divider circuit.

10. A method of controlling a power supply as defined in claim 9 wherein said voltage divider circuit further comprises a plurality of resistors shunted by a respective plurality of transistors, said transistors each controlled by a respective data line of said data bus.

11. A method of controlling a power supply as defined in claim 1 wherein said load further comprises a digital memory circuit.

12. A method of controlling a power supply as defined in claim 11 wherein said digital memory circuit further comprises a flash memory circuit.

13. A method of controlling a power supply as defined in claim 12 further comprising:

storing a portion of said digital data signal as a data word in said flash memory circuit.

14. A method of supplying current to a device having a plurality of data inputs comprising:

sensing a number of zero bits on said plurality of data inputs;

activating a number of charge pump circuits proportional to said number of zero bits;

supplying a level of current to said device proportional to said number of charge pump circuits, whereby said level of current is adapted to meet a requirement of said device related to said number of zero bits.

15. A method of controlling a power supply comprising:

producing an analog signal related to a number of bits having a particular logic state in a digital signal, said analog signal being independent of an output of said power supply;

producing an analog signal related to said number of bits; and

setting an output of said power supply to a particular level in response to said analog signal.

16. A method as defined in claim 15 wherein said power supply comprises a plurality of subcircuits and said setting an output of a power supply comprises:

activating one or more of said subcircuits.

17. A method as defined in claim 16 wherein said subcircuits each include a respective charge pump circuit and wherein said activating one

or more of said subcircuits further comprises enabling a clock circuit connected to drive said respective charge pump circuit.

18. A method of supplying power to a plurality of memory cells of a memory integrated circuit comprising:

sensing a number of zero bits to be written to a corresponding number of said plurality of memory cells; and

activating one or more power supplies in relation to said sensed number of zero bits.

19. A method of controlling a charge pump comprising:

predicting a required level of current;

activating a portion of a multi-portion charge pump so as to supply said required level of current to an output of the charge pump.

20. A method as defined in claim 19 wherein said predicting a required level of current further comprises:

sensing an input to a flash memory device;

determining a required level of programming current based on said input and a known characteristic of said device.

21. A method as defined in claim 20 wherein said input further comprises:

a digital data signal at a data input of said device.

22. A method as defined in claim 20 wherein said known characteristic of said device further comprises a known programming current per memory cell.

23. A method as defined in claim 19 wherein said predicting a required level of current further comprises:

sensing a plurality of input signals on a data bus operatively connected to a device, said data bus having a respective plurality of data bit lines;

determining a number of said plurality of input signals corresponding to a first data state;

predicting said required level of current equal to said number multiplied by a predefined quantity of current.

24. A method of controlling a power supply comprising:

sensing a number of bits in a particular logic state in a particular digital communication; and

adapting said power supply to supply a particular level of current, said level of current being proportional to said number of bits.

25. A method as defined in claim 24 wherein said adapting said power supply further comprises:

switchingly connecting one or more of a plurality of power supply portions to a load circuit.

26. A method as defined in claim 25, wherein said plurality of power supply portions comprises:

a charge pump circuit.

27. An open loop charge pump control method comprising:

providing a plurality of charge pumps, said plurality of charge pumps each adapted to be switchingly connected to an electrical load to supply said electrical load with electrical power;

sensing a data input, said data input adapted to control said electrical load;

switchingly connecting one or more of said plurality of charge pumps in response to said data input, as sensed; and

operating said electrical load so as to draw a level of current within a particular range of currents from said one or more of said switchingly connected plurality of charge pumps.

28. An open loop charge pump control method as defined in claim 27 wherein said sensing a data input further comprises sensing a plurality of data states on a respective plurality of data input lines.

29. An open loop charge pump control method as defined in claim 27, wherein said sensing a data input further comprises sensing a plurality of data states of a serial data transmission.

30. A method as defined in claim 27, wherein said electrical load comprises a portion of a memory integrated circuit.

31. A method as defined in claim 30, wherein said memory integrated circuit comprises a flash memory integrated circuit.

32. An open loop charge pump control method comprising:

providing a plurality of charge pumps, said plurality of charge pump each operatively connected to an electrical load to supply said electrical load with electrical power;

sensing a data input, said data input being operatively connected to said electrical load;

turning on one of said plurality of charge pumps in response to said data input; and

operating said electrical load so as to draw a level of current affected by said turning on of said one charge pump.

33. A charge pump apparatus comprising:

means for sensing a number of bits of a data input having a particular state;

a plurality of charge pump circuits; and

means for activating one or more of said plurality of charge pumps circuits based on said number of bits of data having said particular state, whereby said charge pump apparatus is adapted to provide a particular amount of power to a load circuit.

34. A charge pump apparatus as defined in claim 33 wherein said means for sensing a number of bits comprises digital sensing means.

35. A charge pump apparatus as defined in claim 33 wherein said means for sensing a number of bits comprises analog sensing means.

36. A power supply apparatus comprising:

a plurality of charge pump circuits;

a control circuit having a data input and a control output, said control output being operatively connected to one of said plurality of charge

pump circuits, said control circuit adapted to activate said one of said plurality of charge pump circuits in response to a signal on said data input.

37. A power supply apparatus comprising:

a plurality of charge pump circuits;

an input bus having a plurality of input lines;

a control circuit connected to said input bus, said control circuit adapted to provide a particular plurality of output signals in response to a number of zero bits in an input signal transmitted on said input lines;

a plurality of outputs of said control circuit, said plurality of outputs being operatively connected to said plurality of charge pump circuits respectively, said outputs being adapted to transmit said plurality of output signals to said plurality of charge pumps respectively, whereby said plurality of charge pump are each activated or deactivated in response to said respective plurality of output signals.

38. A memory integrated circuit comprising:

a plurality of memory cells each adapted to be programmed into a respective plurality of logic states;

a plurality of data lines adapted to convey a plurality of data signals to said plurality of memory cells respectively, said data signals corresponding to said logic states respectively;

a control system adapted to sense said plurality of data signals;

a plurality of charge pump circuits operatively connected to said control system and adapted to be controlled by said control system; and

a plurality of conductors adapted to conduct power from said charge pump circuits to said memory cells.

39. A power supply controller comprising:

a plurality of data bus inputs;

a plurality of outputs; and

a sensing circuit adapted to activate one or more of said plurality of outputs in response to a corresponding pattern of data bus signals detected on said plurality of data bus inputs.

40. A power supply controller according to claim 39, wherein said power supply controller further comprises a charge pump circuit connected to one of said plurality of outputs.

41. A processing system comprising:

a microprocessor;

a data bus, said data bus connected to said microprocessor; and

an electronic memory device having a plurality of data bus inputs connected to said data bus, said electronic memory device including a power supply controller having a plurality of outputs and a sensing circuit adapted to activate one or more of the plurality of outputs in response to a pattern of data bus signals detected on said plurality of data bus inputs.

42. A processing system according to claim 41 wherein said electronic memory device further comprises a charge pump circuit, said charge pump circuit connected to one of said plurality of outputs.

43. A microprocessor integrated circuit comprising:

a processing portion; and

a memory portion connected to said processing portion by a data bus portion, said memory portion including a power supply and power supply controller, said power supply controller having a plurality of data bus inputs connected to said data bus portion, an output connected to said power supply, and a sensing circuit adapted to activate or deactivate said output in response to a corresponding pattern of data bus signals detected on said plurality of data bus inputs.